National Semiconductor

May 2007

LM4951 Boomer® Audio Power Amplifier Series
Wide Voltage Range 1.8 Watt Audio Amplifier

General Description

The LM4951 is an audio power amplifier primarily designed for demanding applications in Portable Handheld devices. It is capable of delivering 1.8W mono BTL to an 8Ω load, continuous average power, with less than 1% distortion (THD+N) from a $7.5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4951 does not require bootstrap capacitors, or snubber circuits.

The LM4951 features a low-power consumption active-low shutdown mode. Additionally, the LM4951 features an internal thermal shutdown protection mechanism.

The LM4951 contains advanced pop & click circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4951 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Wide Voltage Range 2.7V to 9V
- Quiescent Power Supply Current (V_{DD} = 7.5V) 2.5mA (typ)
- Power Output BTL at 7.5V, 1% THD 1.8W (typ)
- Shutdown Current 0.01µA (typ)
- Fast Turn on Time 25ms (typ)

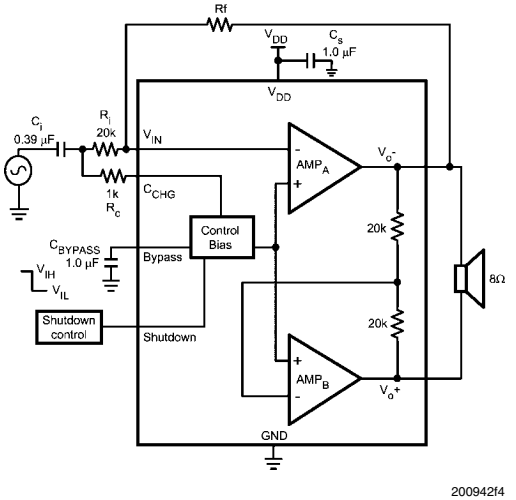
Features

- Pop & click circuitry eliminates noise during turn-on and turn-off transitions
- Low current, active-low shutdown mode
- Low quiescent current
- Thermal shutdown protection
- Unity-gain stable
- External gain configuration capability

Applications

- Portable Handheld Devices up to 9V
- Cell Phone
- PDA

Typical Application

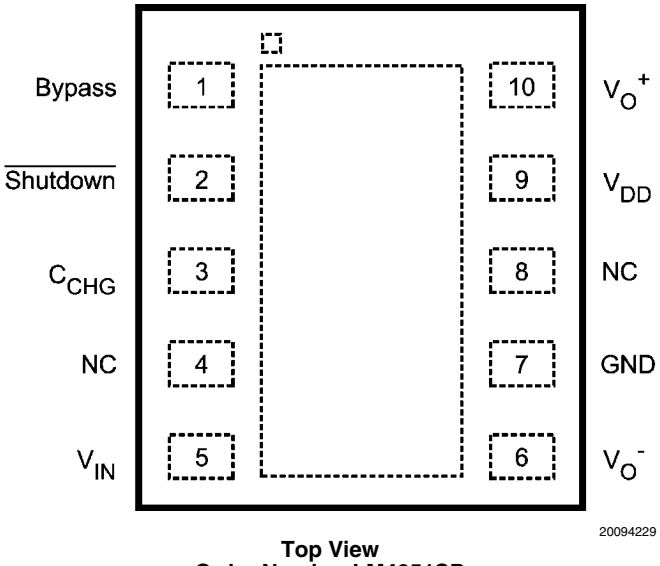


* R_C is needed for over/under voltage protection. If inputs are less than V_{DD} +0.3V and greater than –0.3V, and if inputs are disabled when in shutdown mode, then R_C may be shorted.

FIGURE 1. Typical Bridge-Tied-Load (BTL) Audio Amplifier Application Circuit

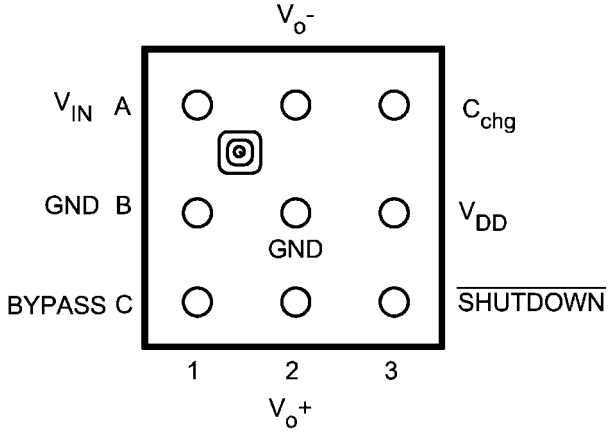
Connection Diagrams

SD Package



Top View
Order Number LM4951SD
See NS Package Number SDC10A

9 Bump micro SMD Package



Top View
Order Number LM4951TL, TLX
See NS Package Number TLA09ZZA

* DAP can either be soldered to GND or left floating.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	9.5V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (LLP) (Note 3)	73°C/W

See AN-1187 'Leadless Leadframe Packaging (LLP).'

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	$2.7V \le V_{DD} \le 9V$

Electrical Characteristics V_{DD} = 7.5V (Notes 1, 2)

The following specifications apply for V_{DD} = 7.5V, $A_{V\text{-}BTL}$ = 6dB, R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4951		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A,RL = 8Ω	2.5	4.5	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND (Note 9)	0.01	5	µA (max)
V_{OS}	Offset Voltage		5	30	mV (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
Rpulldown	Pulldown Resistor on S/D		75	45	kΩ (min)
T_{WU}	Wake-up Time	C_B = 1.0µF	25	35	ms
Tsd	Shutdown time	C_B = 1.0µF		10	ms (max)
TSD	Thermal Shutdown Temperature		170	150 190	°C (min) °C (max)
P_O	Output Power	THD = 1% (max); f = 1kHz R_L = 8Ω Mono BTL	1.8	1.5	W (min)
THD+N	Total Harmomic Distortion + Noise	P_O = 600mWrms; f = 1kHz $A_{V\text{-}BTL}$ = 6dB	0.07	0.5	% (max)
THD+N	Total Harmomic Distortion + Noise	P_O = 600mWrms; f = 1kHz $A_{V\text{-}BTL}$ = 26dB	0.35		%
ε_{OS}	Output Noise	A-Weighted Filter, $R_i = R_f$ = 20kΩ Input Referred, Note 10	10		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200m$V_{p\text{-}p}$, f = 217Hz, C_B = 1.0µF, Input Referred	66	56	dB (min)

Electrical Characteristics V_{DD} = 3.3V (Notes 1, 2)

The following specifications apply for V_{DD} = 3.3V, $A_{V\text{-}BTL}$ = 6dB, R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4951		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A,RL = 8Ω	2.5	4.5	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND (Note 9)	0.01	2	µA (max)
V_{OS}	Offset Voltage		3	30	mV (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 1.0µF	25		ms (max)
Tsd	Shutdown time	C_B = 1.0µF		10	ms (max)
P_O	Output Power	THD = 1% (max); f = 1kHz R_L = 8Ω Mono BTL	280	230	mW (min)

Symbol	Parameter	Conditions	LM4951		Units (Limits)
			Typical (Note 6)	Limit (Notes 7, 8)	
THD+N	Total Harmomic Distortion + Noise1	P_O = 100mWrms; f = 1kHz A_{V-BTL} = 6dB	0.07	0.5	% (max)
THD+N	Total Harmomic Distortion + Noise1	P_O = 100mWrms; f = 1kHz A_{V-BTL} = 26dB	0.35		%
ε_{OS}	Output Noise	A-Weighted Filter, $R_i = R_f$ = 20kΩ Input Referred, Note 10	10		μV
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV_{p-p}$, f = 217Hz, C_B = 1μF, Input Referred	71	61	dB (min)

Note 1: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in Absolute Maximum Ratings, whichever is lower. For the LM4951 typical application (shown in *Figure 1*) with V_{DD} = 7.5V, R_L = 8Ω mono-BTL operation the max power dissipation is 1.42W. θ_{JA} = 73°C/W.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

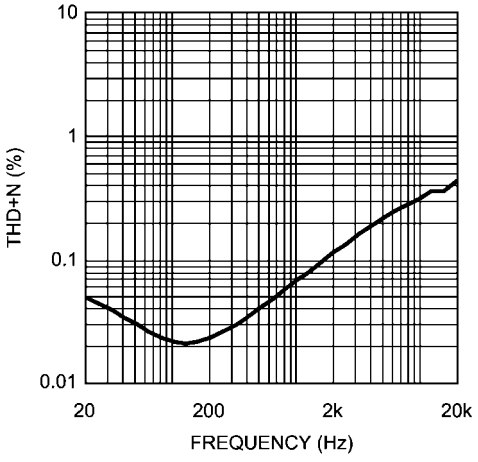
Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: Shutdown current is measured in a normal room environment. The Shutdown pin should be driven as close as possible to GND for minimum shutdown current.

Note 10: Noise measurements are dependent on the absolute values of the closed loop gain setting resistors (input and feedback resistors).

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 3.3V, P_O = 100mW, A_V = 6dB



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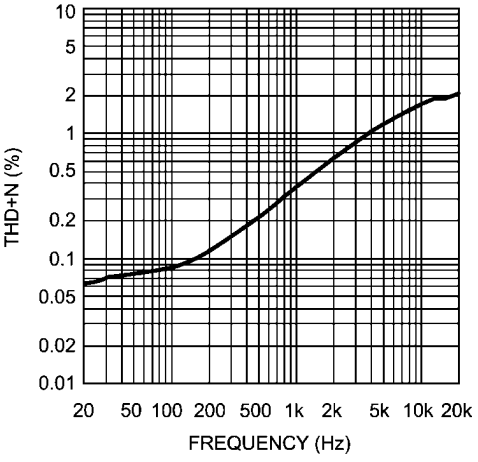
THD+N vs Frequency
V_{DD} = 3.3V, P_O = 100mW, A_V = 26dB



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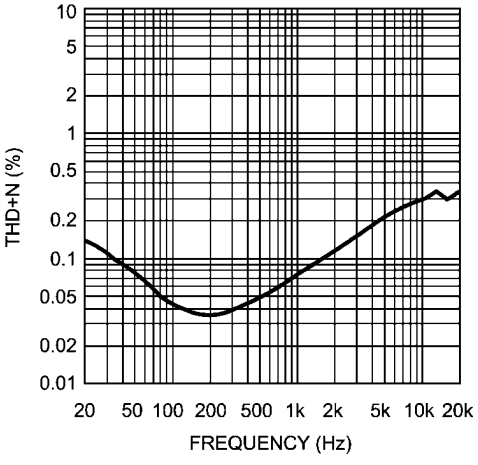
THD+N vs Frequency
V_{DD} = 5V, P_O = 400mW, A_V = 6dB



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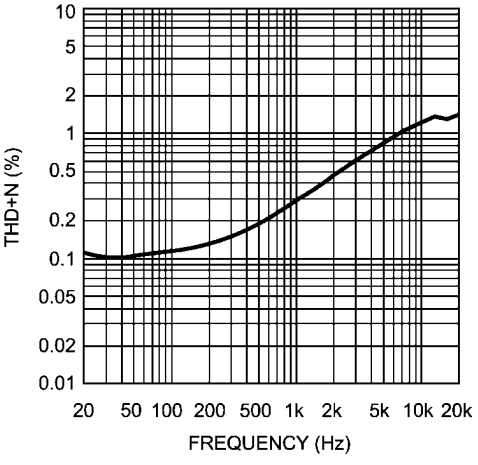
THD+N vs Frequency
V_{DD} = 5V, P_O = 400mW, A_V = 26dB



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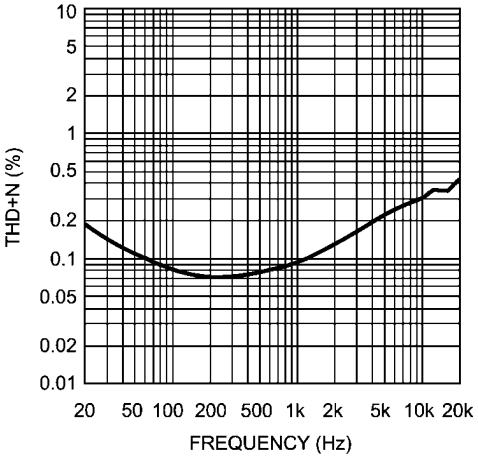
THD+N vs Frequency
V_{DD} = 7.5V, P_O = 600mW, A_V = 6dB



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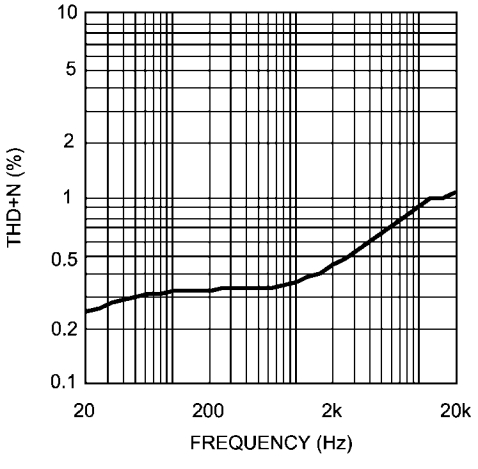
THD+N vs Frequency
V_{DD} = 7.5V, P_O = 600mW, A_V = 26dB



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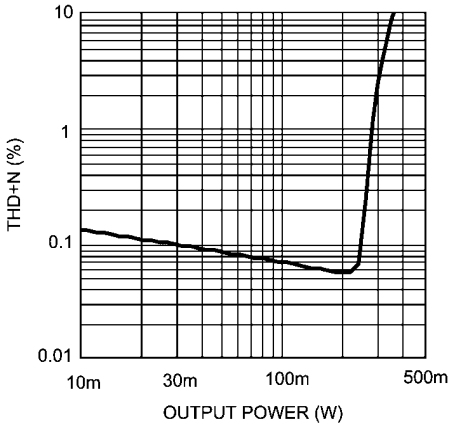
THD+N vs Output Power
V_{DD} = 3.3V, f = 1kHz, A_V = 6dB



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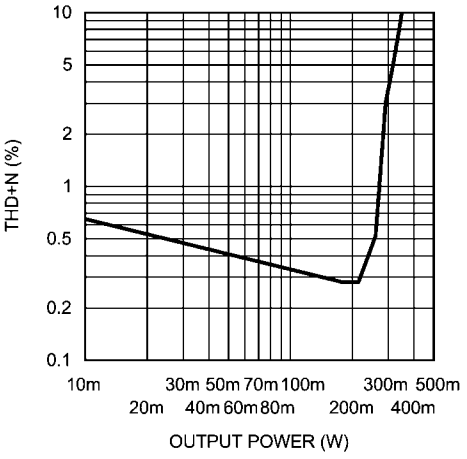
THD+N vs Output Power
V_{DD} = 3.3V, f = 1kHz, A_V = 26dB



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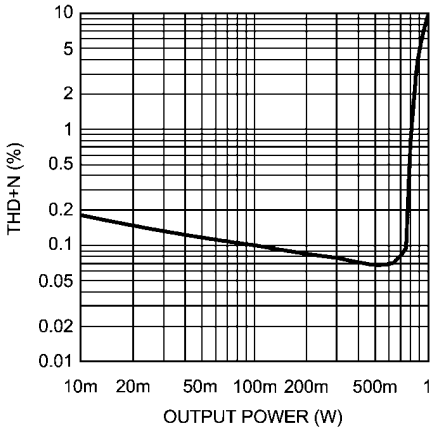
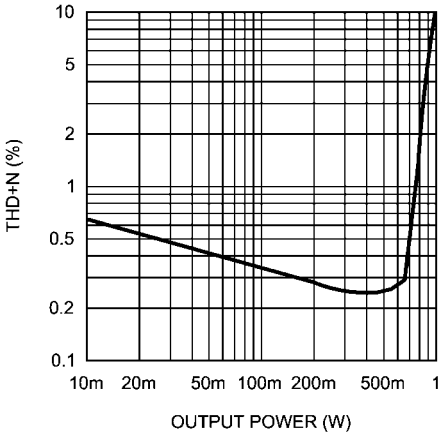
THD+N vs Output Power
V_{DD} = 5V, f = 1kHz, A_V = 6dB



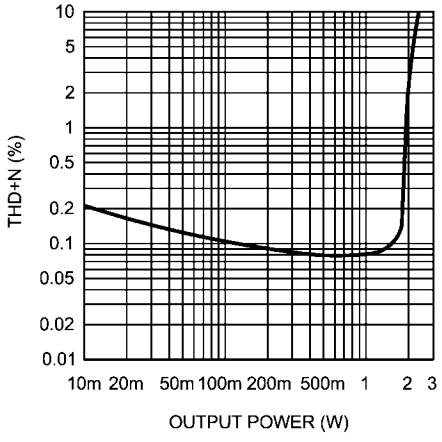
20094209

THD+N vs Output Power
V_{DD} = 5V, f = 1kHz, A_V = 26dB



20094210

THD+N vs Output Power
V_{DD} = 7.5V, f = 1kHz, A_V = 6dB



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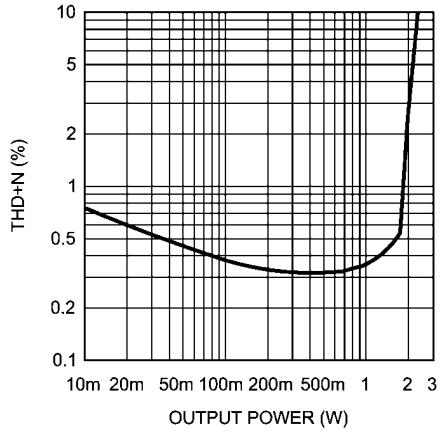
THD+N vs Output Power
V_{DD} = 7.5V, f = 1kHz, A_V = 26dB



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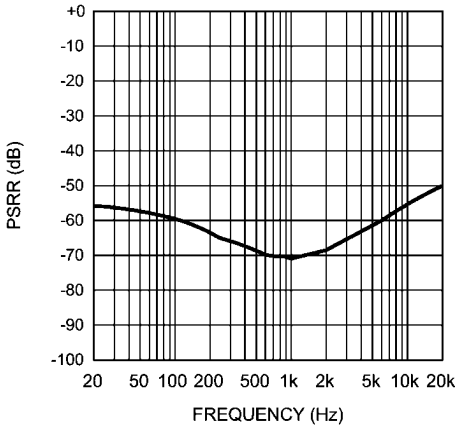
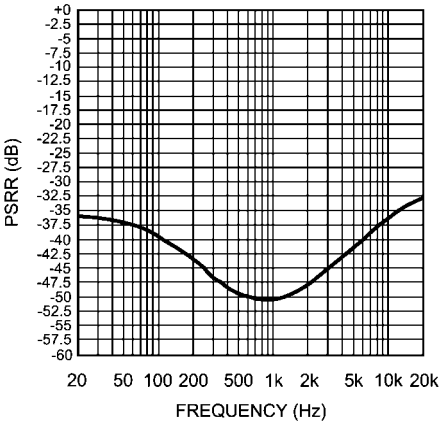
Power Supply Rejection vs Frequency
V_{DD} = 3.3V, A_V = 6dB, V_{RIPPLE} = 200mV_{P-P}
Input Terminated into 10Ω



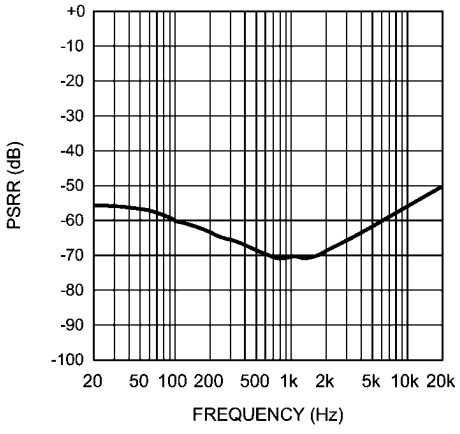
20094213

Power Supply Rejection vs Frequency
V_{DD} = 3.3V, A_V = 26dB, V_{RIPPLE} = 200mV_{P-P}
Input Terminated into 10Ω



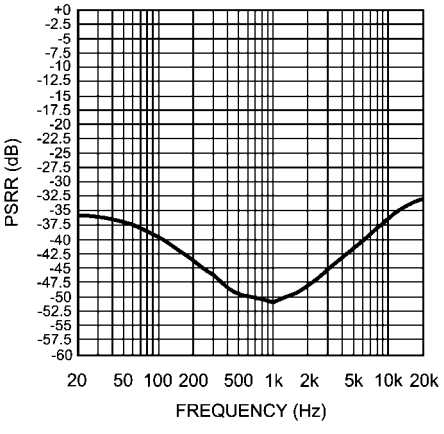
20094214

Power Supply Rejection vs Frequency
V_{DD} = 5V, A_V = 6dB, V_{RIPPLE} = 200mV_{P-P}
Input Terminated into 10Ω



20094215

Power Supply Rejection vs Frequency
V_{DD} = 5V, A_V = 26dB, V_{RIPPLE} = 200mV_{P-P}
Input Terminated into 10Ω



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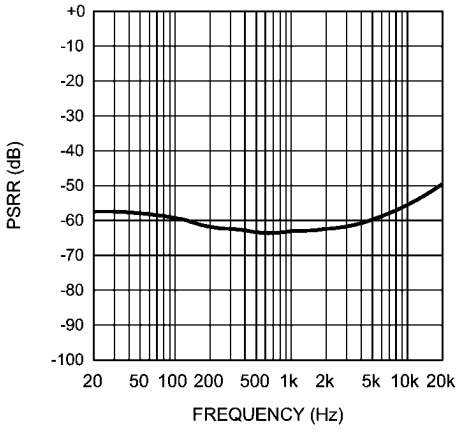
Power Supply Rejection vs Frequency
V_{DD} = 7.5V, A_V = 6dB, V_{RIPPLE} = 200mV_{P-P}
Input Terminated into 10Ω



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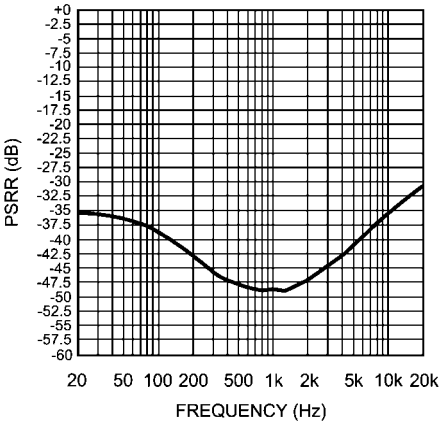
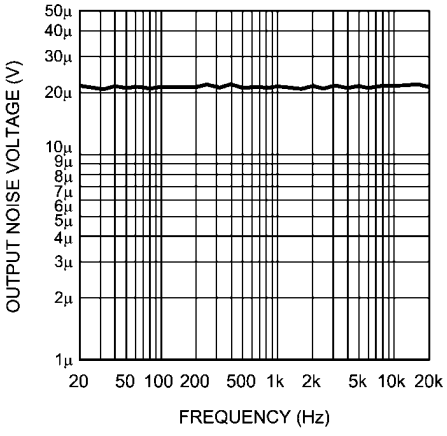
Power Supply Rejection vs Frequency
V_{DD} = 7.5V, A_V = 26dB, V_{RIPPLE} = 200mV_{P-P}
Input Terminated into 10Ω



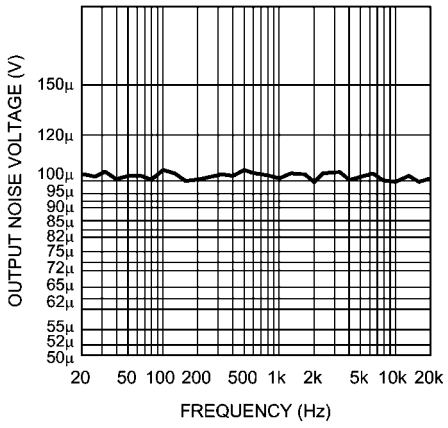
20094218

Noise Floor
V_{DD} = 3.3V, A_V = 6dB, R_i = R_f = 20kΩ
BW < 80kHz, A-weighted



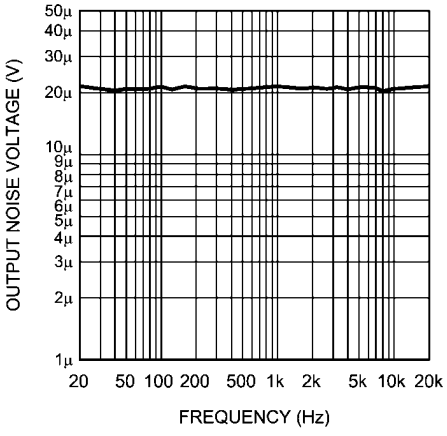
20094219

Noise Floor
V_{DD} = 3V, A_V = 26dB, R_i = 20kΩ, R_f = 200kΩ
BW < 80kHz, A-weighted



20094220

Noise Floor
V_{DD} = 5V, A_V = 6dB, R_i = R_f = 20kΩ
BW < 80kHz, A-weighted



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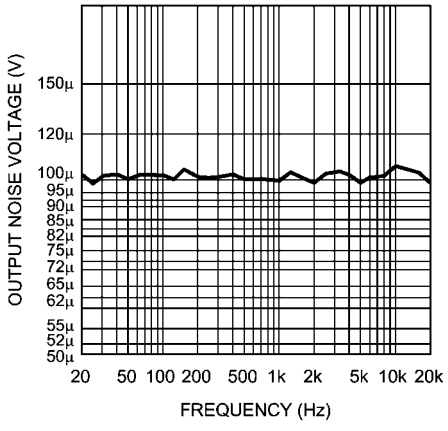
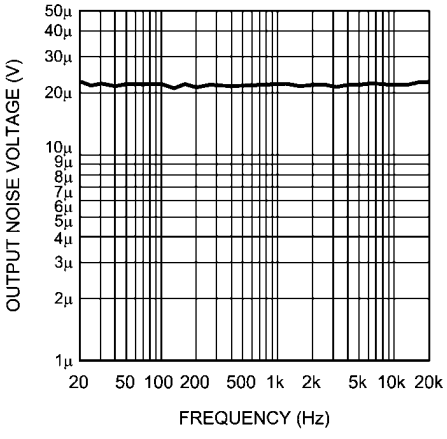
Noise Floor
V_{DD} = 5V, A_V = 26dB, R_i = 20kΩ, R_f = 200kΩ
BW < 80kHz, A-weighted



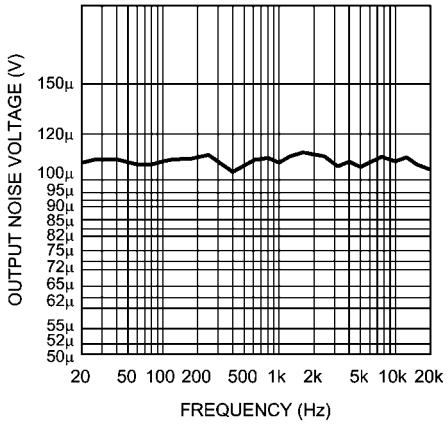
20094222

Noise Floor
V_{DD} = 7.5V, A_V = 6dB, R_i = R_f = 20kΩ
BW < 80kHz, A-weighted



20094223

Noise Floor
V_{DD} = 7.5V, A_V = 26dB, R_i = 20kΩ, R_f = 200kΩ
BW < 80kHz, A-weighted



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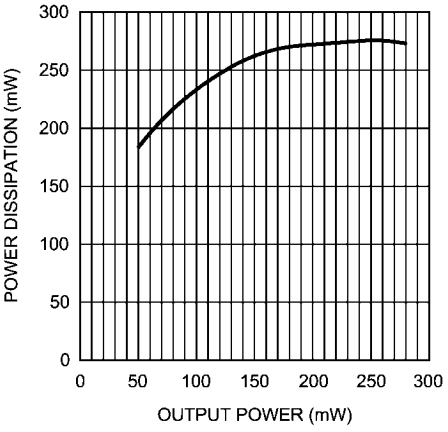
Power Dissipation vs Output Power
V_{DD} = 3.3V, R_L = 8Ω, f = 1kHz



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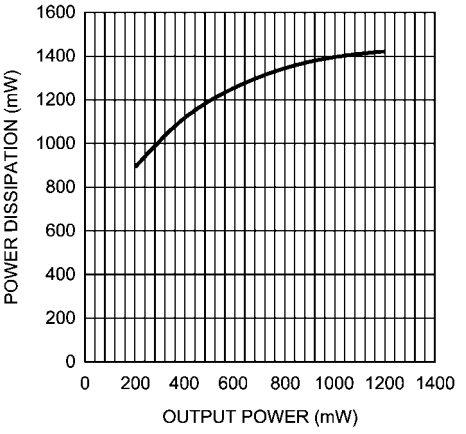
Power Dissipation vs Output Power
V_{DD} = 7.5V, R_L = 8Ω, f = 1kHz



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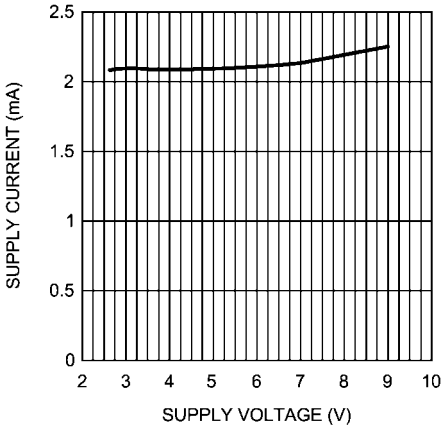
Supply Current vs Supply Voltage
R_L = 8Ω, V_{IN} = 0V, R_{source} = 50Ω



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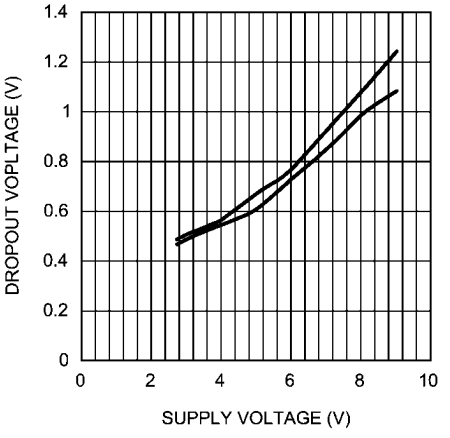
Clipping Voltage vs Supply Voltage
R_L = 8Ω,
from top to bottom: Negative Voltage Swing; Positive Voltage Swing



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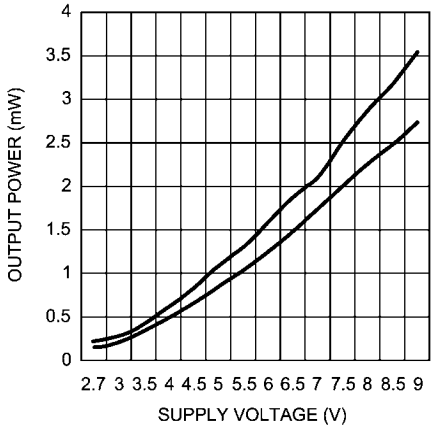
Output Power vs Supply Voltage
R_L = 8Ω,
from top to bottom: THD+N = 10%, THD+N = 1%



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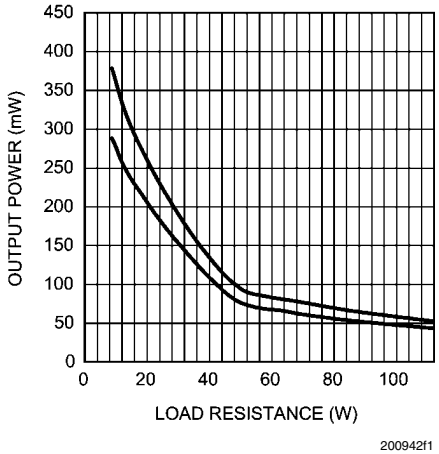
Output Power vs Load Resistance
V_{DD} = 3.3V, f = 1kHz
from top to bottom: THD+N = 10%, THD+N = 1%



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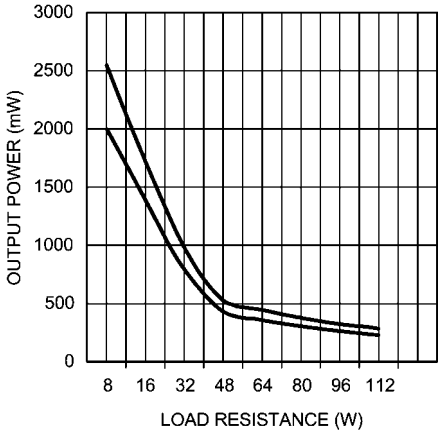
Output Power vs Load Resistance
V_{DD} = 7.5V, f = 1kHz
from top to bottom: THD+N = 10%, THD+N = 1%



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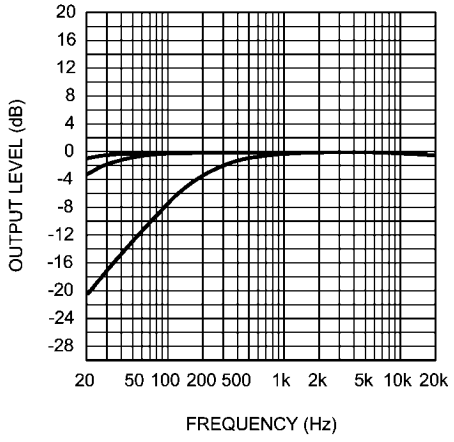
Frequency Response vs Input Capacitor Size
R_L = 8Ω
from top to bottom: C_i = 1.0µF, C_i = 0.39µF, C_i = 0.039µF



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Application Information

HIGH VOLTAGE BOOMER

Unlike previous 5V Boomer® amplifiers, the LM4951 is designed to operate over a power supply voltages range of 2.7V to 9V. Operating on a 7.5V power supply, the LM4951 will deliver 1.8W into an 8Ω BTL load with no more than 1% THD +N.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4951 consists of two operational amplifiers that drive a speaker connected between their outputs. The value of input and feedback resistors determine the gain of each amplifier. External resistors R_i and R_f set the closed-loop gain of AMP_A, whereas two 20kΩ internal resistors set AMP_B's gain to -1. The LM4951 drives a load, such as a speaker, connected between the two amplifier outputs, V_O+ and V_O -. Figure 1 shows that AMP_A's output serves as AMP_B's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between AMP_A and AMP_B and driven differentially (commonly referred to as "bridge mode"). This results in a differential, or BTL, gain of

$$A_{VD} = 2(R_f / R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the **AUDIO POWER AMPLIFIER DESIGN** section. Under rare conditions, with unique combinations of high power supply voltage and high closed loop gain settings, the LM4951 may exhibit low frequency oscillations.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing AMP1's and AMP2's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful bridged amplifier.

The LM4951's dissipation when driving a BTL load is given by Equation (2). For a 7.5V supply and a single 8Ω BTL load, the dissipation is 1.42W.

$$P_{DMAX-MONOBTL} = 4(V_{DD})^2 / 2\pi^2 R_L: \quad \text{Bridge Mode} \quad (2)$$

The maximum power dissipation point given by Equation (2) must not exceed the power dissipation given by Equation (3):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (3)$$

The LM4951's T_{JMAX} = 150°C. In the SD package, the LM4951's θ_{JA} is 73°C/W when the metal tab is soldered to a copper plane of at least 1in². This plane can be split between the top and bottom layers of a two-sided PCB. Connect the two layers together under the tab with an array of vias. At any given ambient temperature T_A, use Equation (3) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (3) and substituting P_{DMAX} for P_{DMAX}' results in Equation (4). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4951's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-MONOBTL}\theta_{JA} \quad (4)$$

For a typical application with a 7.5V power supply and a BTL 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 46°C for the TS package.

$$T_{JMAX} = P_{DMAX-MONOBTL}\theta_{JA} + T_A \quad (5)$$

Equation (5) gives the maximum junction temperature T_{JMAX}. If the result violates the LM4951's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. Further, ensure that speakers rated at a nominal 8Ω do not fall below 6Ω. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pins, supply pin and amplifier output pins. Refer to the **Typical Performance Characteristics** curves for power dissipation information at lower output power levels.

POWER SUPPLY VOLTAGE LIMITS

Continuous proper operation is ensured by never exceeding the voltage applied to any pin, with respect to ground, as listed in the Absolute Maximum Ratings section.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a voltage regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4951's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the LM4951's power supply pin and ground as short as possible.

Connecting a larger capacitor, C_{BYPASS}, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_{BYPASS}, depends on desired PSRR requirements, click and pop performance (as explained in the section, **SELECTING EXTERNAL COMPONENTS**), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The LM4951 features an active-low micro-power shutdown mode. When active, the LM4951's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.01µA typical shutdown current is achieved by applying a voltage to the SHUTDOWN pin that is as near to GND as possible. A voltage that is greater than GND may increase the shutdown current.

There are a few methods to control the micro-power shutdown. These include using a single-pole, single-throw switch (SPST), a microprocessor, or a microcontroller. When using a switch, connect the SPST switch between the shutdown pin and V_{DD}. Select normal amplifier operation by closing the switch. Opening the switch applies GND to the SHUTDOWN pin activating micro-power shutdwon.The switch and internal pull-down resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the active-state voltage to the SHUTDOWN pin.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Two quantities determine the value of the input coupling capacitor: the lowest audio frequency that requires amplification and desired output transient suppression.

As shown in Figure 1, the input resistor (R_i) and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation (6).

$$f_c = 1/2\pi R_i C_i \quad (6)$$

As an example when using a speaker with a low frequency limit of 50Hz, C_i, using Equation (6) is 0.159µF. The 0.39µF C_{INA} shown in Figure 1 allows the LM4951 to drive high efficiency, full range speaker whose response extends below 30Hz.

Selecting Value For R_C

The LM4951 is designed for very fast turn on time. The Cchg pin allows the input capacitors (CinA and CinB) to charge quickly to improve click/pop performance. Rchg1 and Rchg2 protect the Cchg pins from any over/under voltage conditions caused by excessive input signal or an active input signal when the device is in shutdown. The recommended value for Rchg1 and Rchg2 is 1kΩ. If the input signal is less than V_{DD} +0.3V and greater than -0.3V, and if the input signal is disabled when in shutdown mode, Rchg1 and Rchg2 may be shorted out.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4951 contains circuitry that eliminates turn-on and shutdown transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated.

As the $V_{DD}/2$ voltage present at the BYPASS pin ramps to its final value, the LM4951's internal amplifiers are configured as unity gain buffers. An internal current source charges the capacitor connected between the BYPASS pin and GND in a controlled manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin.

The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches $V_{DD}/2$. As soon as the voltage on the bypass pin is stable, there is a delay to prevent undesirable output transients (“click and pops”). After this delay, the device becomes fully functional.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1.8W into an 8Ω BTL

The following are the desired operational parameters:

Power Output	$1.8W_{RMS}$
Load Impedance	8Ω
Input Level	$0.3V_{RMS}$ (max)
Input Impedance	20kΩ
Bandwidth	50Hz–20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the *Output Power vs Power Supply Voltage* curve in the **Typical Performance Characteristics** section. Another way, using Equation (7), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the *Clipping Dropout Voltage vs Power Supply Voltage* in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (7). The result is Equation (8).

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (7)$$

$$V_{DD} = V_{OUTPEAK} + V_{ODTOP} + V_{ODBOT} \quad (8)$$

The commonly used 7.5V supply voltage easily meets this. The additional voltage creates the benefit of headroom, allowing the LM4951 to produce peak output power in excess of 1.8W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the Power Dissipation section. After satisfying the LM4951's power dissipation requirements, the minimum differential gain needed to achieve 1.8W dissipation in an 8Ω BTL load is found using Equation (9).

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (9)$$

Thus, a minimum gain of 12.6 allows the LM4951's to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_{V\text{-}BTL}$ = 13. The amplifier's overall BTL gain is set using the input (R_i) and feedback (R_f) resistors of the first amplifier in the series BTL configuration. Additionaly, $A_{V\text{-}BTL}$ is twice the gain set by the first amplifier's R_i and R_f. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (10).

$$R_f / R_i = A_{V\text{-}BTL} / 2 \quad (10)$$

The value of R_f is 130kΩ (choose 191kΩ, the closest value). The nominal output power is 1.8W.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB-desired limit. The results are an

$$f_L = 50Hz / 5 = 10Hz \quad (11)$$

and an

$$f_L = 20kHz \times 5 = 100kHz \quad (12)$$

As mentioned in the **SELECTING EXTERNAL COMPONENTS** section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (13).

$$C_i = 1 / 2\pi R_i f_L \quad (13)$$

The result is

$$1 / (2\pi \times 20k\Omega \times 10Hz) = 0.795\mu F$$

Use a 0.82µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain A_{VD}, determines the upper passband response limit. With $A_{VD} = 7$ and $f_H = 100kHz$, the closed-loop gain bandwidth product (GBWP) is 700kHz. This is less than the LM4951's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figures 2–4 show the recommended two-layer PC board layout that is optimized for the SD10A. This circuit is designed for use with an external 7.5V supply 8Ω (min) speakers.

These circuit boards are easy to use. Apply 7.5V and ground to the board's V_{DD} and GND pads, respectively. Connect a speaker between the board's OUT_A and OUT_B outputs.

Demonstration Board Layout

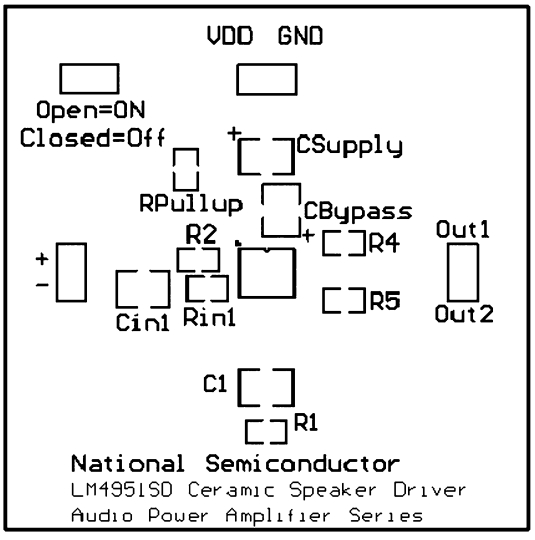

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FIGURE 2. Recommended TS SE PCB Layout: Top Silkscreen

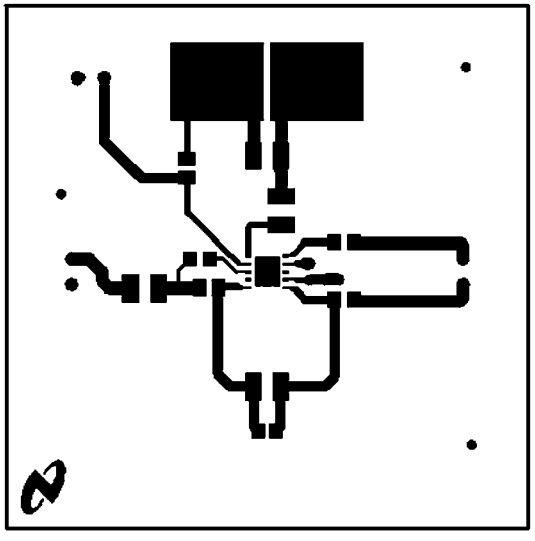

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FIGURE 3. Recommended TS SE PCB Layout: Top Layer

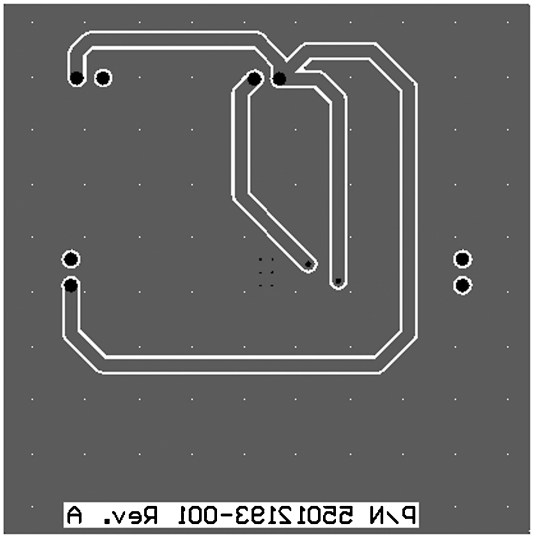

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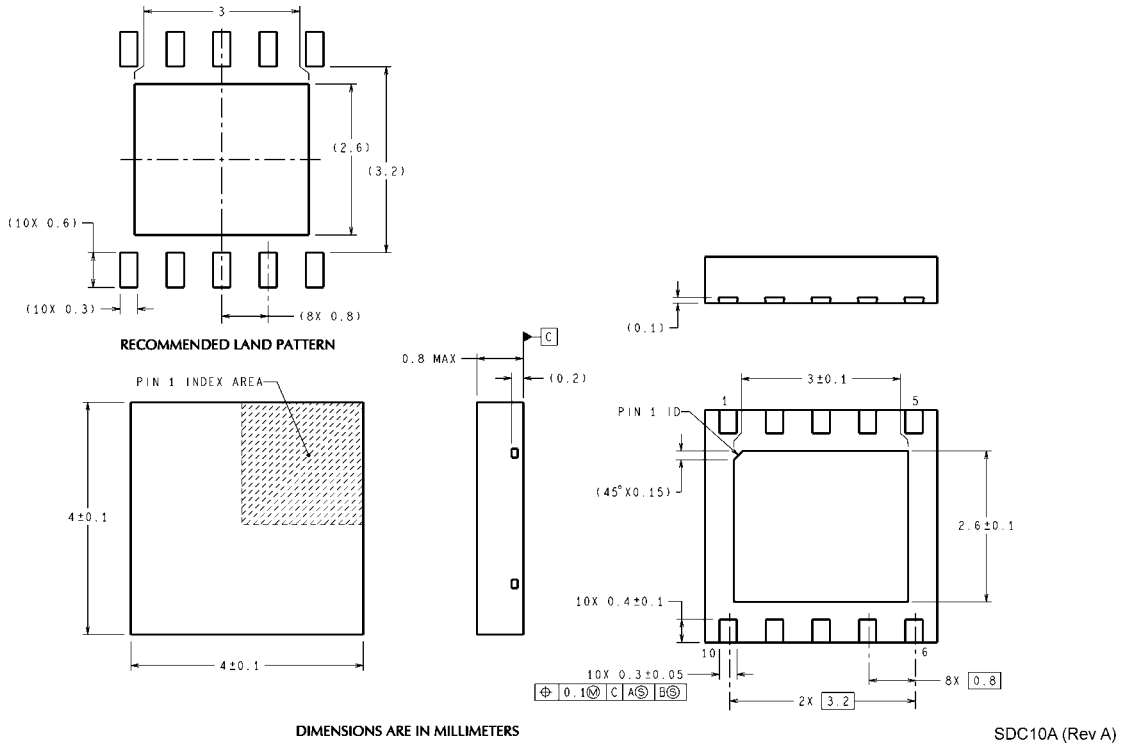
FIGURE 4. Recommended TS SE PCB Layout: Bottom Layer

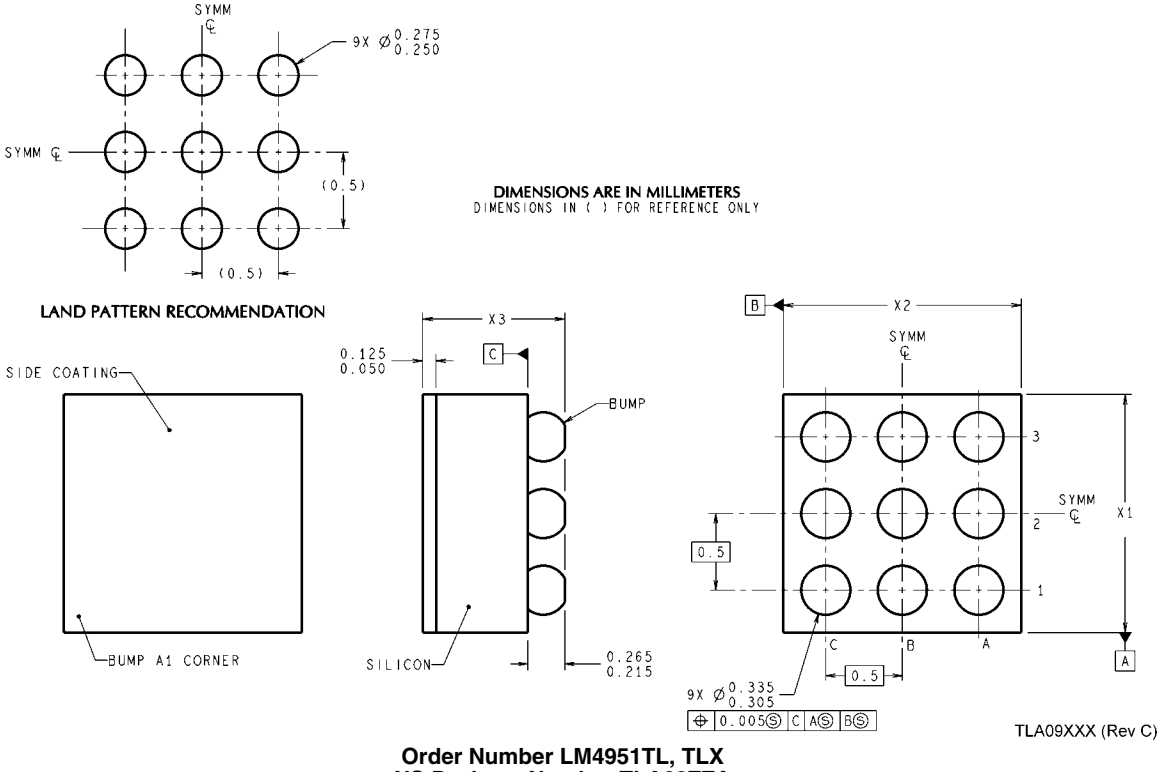
Revision History

Rev	Date	Description
1.0	8/25/04	Initial WEB.
1.1	10/19/05	Added the micro SMD pkg, then WEB.
1.2	08/30/06	Added the Limit value (=35) on the Twu (7.5V Elect Char table), then WEB.
1.3	09/11/06	Added the “Selecting Value For Rc, then WEB.
1.4	05/21/07	Fixed a typo (X3 value = 0.600±0.075) instead of (X3 = 0.600±0.75).

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM4951SD
NS Package Number SDC10A



Order Number LM4951TL, TLX
NS Package Number TLA09ZZA
X_1 = 1.463±0.03, X_2 = 1.463±0.03, X_3 = 0.600±0.075

Notes

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